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Investigation of Lateral RESURF, 6H-SiC MOSFETs

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Abstract: We report on theoretical and experimental investigations of 600 V, lateral RESURF, 6H-SiC MOSFETs. The 2 dimensional device simulations show that the breakdown voltage of this class of devices is limited by the peak electric field in the oxide, which should be kept below 3 MV/cm for long-term reliability. The devices made on 6H-SiC substrates show 600 V breakdown, which was limited by the breakdown of the gate oxide. In order to reduce the electric field in the gate oxide, we show that it is necessary to reduce the doping of the lateral drift layer. This results in excessive specific on-resistance, which is dominated by the resistance of the drift layer. The inversion layer electron mobility of 50-60 $cm^2/V{\cdot}s$ was obtained on experimental devices. Large area devices (560 μm x 1700 μm) had a specific on-resistance of 57 $mohm{\cdot}cm^2$.

Introduction: Both vertical and lateral power MOSFETs in 6H- and 4H-SiC have been reported [1-6]. The overall goal is to develop a MOS process technology in SiC having a gate insulator with a high quality SiC/SiO_2 interface, high electron inversion layer mobility, low interface trap density, appropriate lateral drift layer, good contacts, and high conductivity of the source and drain regions. These requirements are often conflicting. For example, the high temperature required for activation of various implants can lead to surface roughness resulting in poor inversion layer electron mobility. In our previous work [7], the source/drain and drift layer implants were activated at 1200°C which caused insufficient activation, very high sheet resistance of the source/drain regions and poor mobility in the drift region due to the residual implant damage. In this work, we have activated the implants at 1400°C resulting in much improved activation, lower sheet resistances, theoretical mobility in the drift layer while retaining the high inversion layer electron mobility of 50-60 $cm^2/V{\cdot}s$.

Device Structure: Two different SiC high voltage lateral MOSFET designs are shown in Figs 1-2.

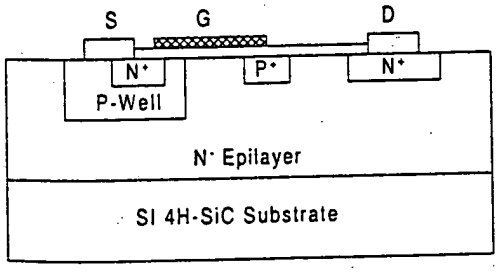

Fig. 1 The conventional LDMOS structure as reported by Purdue University [6].

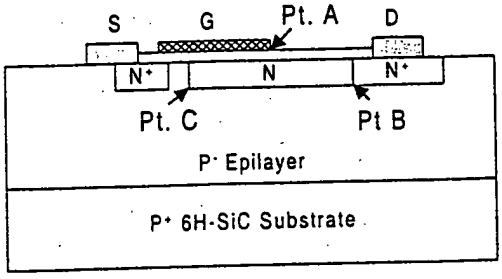

Fig. 2 The LDMOS structure used in this work.

The drawings in Figs 1-2 are oversimplified and do not show field oxide etc. The structure in Fig. 1 was first reported by Purdue Univ.[6]. This structure employs a gate oxide grown on the surface of

a p-well which has to be implanted. A major drawback of this scheme is that it requires >1400° anneal to activate the boron or aluminum implants. Such a high temperature results in surfa roughness leading to poor inversion layer electron mobility. Currently, techniques of reducing t so-called "step-bunching" during implant-activation are being investigated. The second structu avoids the p-well entirely and utilizes the p-epitaxial layer with good surface quality. The implant n-drift layer can be fully activated at 1400°C in 6H-SiC.

Two Dimensional Device Simulations: The structure shown in Fig. 2 was simulated using the 2 device simulator from Siborg Systems Inc. The x-component of the electric field in SiC, E_x(SiC along the line BC in Fig. 2 and the y-component of the electric field in SiO_2, $E_y(SiO_2)$, along th gate electrode/SiO_2 interface are shown in Fig. 3 with drain biased at 600 V. The doping of the 0. μm thick drift layer was $1x10^{17}$ cm^{-3} and the length was 15 μm. The p-type channel doping wa 10^{16} cm^{-3}. Clearly, the field in the oxide peaked at the edge of the polysilicon gate electrod overlapping the n^- drift layer (point A in Fig. 2) and has exceeded 3 MV/cm for a drain voltage c only 600 V. This is a direct result of the fact that $E_y(SiO_2)$ is 2.5x (ratio of dielectric constants c SiC and SiO_2) of E_y(SiC). It should be noted that this problem does not arise in silicon devices, a the maximum breakdown field in Si is 0.4 MV/cm, which limits the electric field in oxide to 1. MV/cm. In order to overcome this problem, the doping density in the drift layer can be selectivel reduced under the gate electrode. In practice, this is costly because it causes the FET resistance t increase. We have done simulations by uniformly reducing the doping density in the drift layer The results are shown in Fig. 4. As expected, $E_y(SiO_2)$ at point A reduces and E_x(SiC) at point E increases with reductions in the drift layer doping at a constant drain bias of 600 V. For drift laye doping above 10^{17} cm^{-3}, the E_x (SiC) peaks at point C instead of point B as expected.

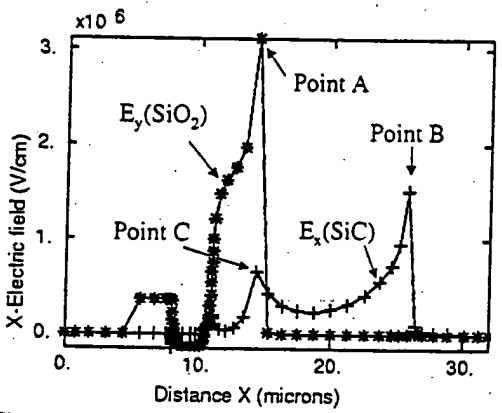

Fig. 3 2D device simulation results of the structure shown in Fig. 2. The drift layer was 15 μm long, 0.5 μm thick, and doped at $1x10^{17}$ cm^{-3}. The gate and source were grounded and the drain was biased at 600 V. The locations of points A, B and C are shown in Fig. 2.

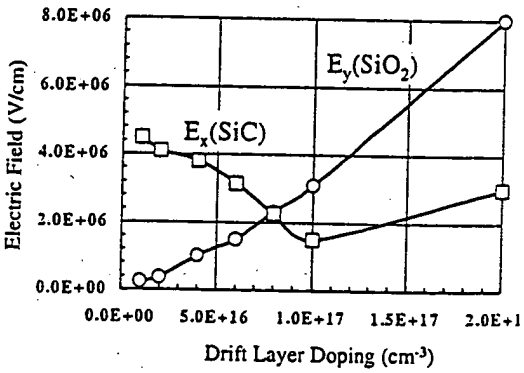

Fig. 4 The variation of $E_y(SiO_2)$ at point A and E_x(SiC) at points B or C with drift layer doping. The reduction of the drift layer doping reduces $E_y(SiO_2)$ but increases E_x(SiC) at point B. The drift layer doping of $1x10^{17}$ cm^{-3} seems to be optimal.

The reduction in the drift layer doping, of course, leads to increase in the specific on-resistance of the MOSFET as shown in Fig. 5. These results are calculated assuming parameters similar to those given in Table 1. The gate voltage was fixed at 10 V. From these simulation results, it is clear that the optimum doping for the drift layer which keeps the peak field in the oxide at or below 3 MV/cm is about $1x10^{17}$ cm^{-3}. Higher doping will cause the oxide to breakdown at point A. Lower doping will cause SiC to breakdown at point B. The total specific resistance for the optimal doping is 38 mohm·cm^2. 50% of which is in the drift layer and the remaining 50% is in the inversion layer.

Device Fabrication: We have implemented the structure shown in Fig. 2 on p^+ 6H-SiC substrates with 10 μm of p-epitaxial layer doped at $1x10^{16}$ cm^{-3}. The device parameters are listed in Table 1. The source, drain and the lateral drift regions were implanted with nitrogen to a depth of 0.5 μm and activated in argon at 1400°C for 30 minutes. The implanted dose in the drift region was $3.75x10^{12}$ cm^{-2} and resulted in a sheet resistance of 6180 ohm/sq. This corresponds to a bulk electron mobility of 270 $cm^2/V{\cdot}s$ along the a-axis, and demonstrates that the 1400°C anneal is sufficient for activation of N implants. At the same time, the temperature is low enough to avoid "step-bunching" on the SiC surface which can drastically reduce the inversion layer electron mobility. The 31 nm thick gate oxide was grown wet at 1100°C for 3 hours and then re-oxidized wet at 950°C for 90 min to obtain a low interface trap density [8]. A thick ~ 7 kÅ field oxide was formed during the same oxidation step by complete oxidation of an un-doped polysilicon layer. A 3.5 kÅ thick layer of polysilicon was deposited and doped with phosphorus at 900°C for the gate electrode. The ohmic contacts to the n^+ source and drain regions were formed by depositing 800Å of nickel annealed at 800°C for 150 s.

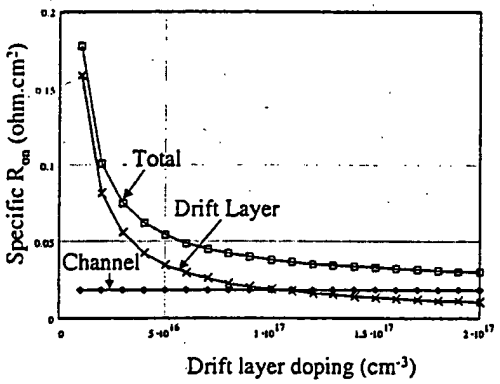

Fig. 5 The calculations of the channel and drift layer components of the specific on resistance for 6H-SiC LDMOS. The device parameters were similar to those shown in Table 1. The gate voltage was fixed at 10 V.

Table 1 Device parameters of the fabricated 6H-SiC LDMOSFET

P epilayer doping (cm^{-3}), thickness (μm)	$1x10^{16}$, 10
Drift layer implanted dose (cm^{-2})	$3.75x10^{12}$
Sheet resistance of the drift layer (ohm/sq)	6180
Sheet resistance of n^+ source/drain (ohm/sq)	695
Contact resistance to n^+ source/drain ($ohm{\cdot}cm^2$)	$1.05x10^{-5}$
Gate oxide thickness (Å)	310
Channel length (μm), drift layer length (μm)	3, 15
Inversion layer electron mobility ($cm^2/V{\cdot}s$)	50-60

Experimental Results: The enclosed RESURF MOSFETs were fabricated with two different drift region lengths (10 and 15 μm) and three different gate lengths (3, 5, and 10 μm). The I-V characteristics for the FET with 10 μm gate length and 15 μm drift region are shown in Fig. 6. This FET broke down at 650 V at point A in Fig. 2. The inversion layer electron mobility (extracted from the long gate length devices without the RESURF region) was 50-60 $cm^2/V{\cdot}s$. A large device with channel length of 3 μm, total periphery of 3 cm and drift length of 10 μm was measured (Fig 7). The measured on-resistance at a gate voltage of 10 V was 57 $mohm{\cdot}cm^2$ (compared to the calculated value of 48 $mohm{\cdot}cm^2$ shown in Fig. 5 corresponding to the drift layer doping of $7.5x10^{16}cm^{-3}$ in the fabricated devices). Of the total series resistance, the dominant source of resistance, 69%, was in the drift layer. ***The gate voltage of 10 V is very reasonable from the standpoint of long-term reliability of the gate oxide.*** The large area inter-digitated devices broke down at around 400-450 V.

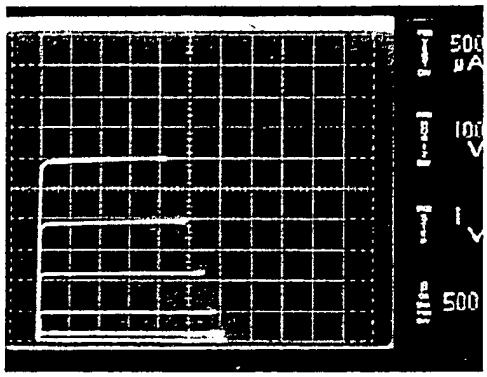

Fig. 6 The I-V characteristics of an enclosed LDMOS with L=10 μm, L_{drift}=15 μm. The gate voltage is from 0 to +5 V.

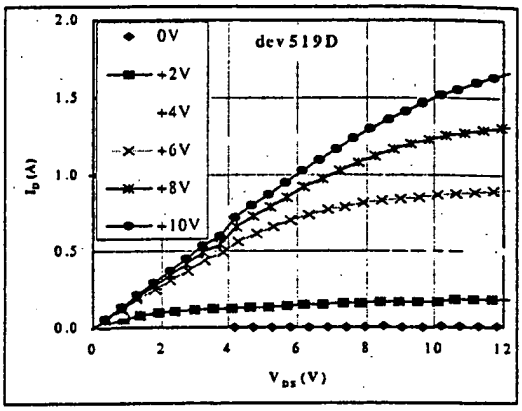

Fig. 7 The forward I-V characteristics of a large area device with L = 3 μm, W = 3 cm, L_{drift} = 10 μm. The active area was 560 μm x 1700 μm.

Summary: Lateral high voltage 6H-SiC MOSFETs have been successfully fabricated using 1400°C implant anneal in Ar ambient. The MOS inversion layer mobility is high enough (50-60 $cm^2/V{\cdot}s$) so that the FET resistance is limited by the resistance of the implanted drift layer, and not the MOS channel resistance, as desired. The measured specific on-resistance is 57 $mohm{\cdot}cm^2$ consistent with the drift layer sheet resistance (6180 ohm/sq). Future work should focus on obtaining higher breakdown voltages consistent with the drift layer design. This may involve optimization of the structure shown in Fig. 1 which has an extra P^+ implant to shield the gate oxide from the high fields.

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References:

[1] J.W. Palmour, J.A. Edmond, H.S. Kong, and C.H. Carter, Jr., Proc. 28th Intersociety Energy Conversion Engineering Conf., Amer. Chem Soc. 1 (1993), p. 249.
[2] A.K. Agarwal, J.B. Casady, L.B. Rowland, W.F. Valek, M.H. White, and C.D. Brandt, IEEE Electron Dev. Letts. 18 (1997), p. 586.
[3] J.N. Shenoy, J.A. Cooper, Jr., and M. R. Melloch, IEEE Electron Dev. Letts. 18 (1997), p. 93.
[4] D. Peters, R. Schorner, P. Friedrichs, J. Volkl, H. Mitlehner, and D. Stephani, IEEE Trans. Electron Devices 46 (1999), p. 542.
[5] P.M. Shenoy and B.J. Baliga, IEEE Electron Dev. Letts. 18 (1997), p. 589.
[6] J. Spitz, M.R. Melloch, J.A. Cooper, Jr., and M.A. Capano, IEEE Electron Dev. Letts. 19 (1998), p. 100.
[7] N. S. Saks, S. S. Mani, A. K. Agarwal, and M. G. Ancona, IEEE Electron Dev. Letts. 20 (1999), p. 431.
[8] L.A. Lipkin, D.B. Slater, Jr., and J.W. Palmour, Mat. Sci. For. 264-8 (1998), p. 853.

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